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[Title of the Invention] LIQUID CRYSTAL DISPLAY DEVICE

[Abstract]

[Purpose] It is possible to form an LDD structure without executing two times of ion implantation and to lower a drain leakage current value.

[Construction] In a liquid crystal display device including at least a thin film transistor (TFT) array substrate having: an insulating substrate; a pixel portion which includes polycrystalline silicon TFTs for switching formed on the substrate; and a driving circuit portion which is formed adjacently to the pixel portion and includes polycrystalline silicon TFTs for driving the pixel portion, the polycrystalline silicon TFTs each have a gate electrode consisting of a two layer structure of an upper layer and a lower layer, an area of the gate electrode of the lower layer is wider than an area of the gate electrode of the upper layer, and a charge concentration of a polycrystalline silicon layer in a region just under the gate electrode consisting of only the lower layer of the lower layer portion wider than the area of the gate electrode of the upper layer is an intermediate concentration of a channel region and a source

or drain region.

[Scope of Claim]

[Claim 1] A liquid crystal display device comprising at least a thin film transistor (TFT) array substrate having: an insulating substrate; a pixel portion which includes polycrystalline silicon TFTs for switching formed on the substrate; and a driving circuit portion which is formed adjacently to the pixel portion and includes polycrystalline silicon TFTs for driving the pixel portion,

characterized in that the polycrystalline silicon TFTs each have a gate electrode consisting of a two layer structure of an upper layer and a lower layer, an area of the gate electrode of the lower layer is wider than the area of the gate electrode of the upper layer, and a charge concentration of a polycrystalline silicon layer in a region just under the gate electrode consisting of only the lower layer of the lower layer portion wider than an area of the gate electrode of the upper layer is an intermediate concentration of a channel region and a source or drain region.

[Detailed Description of the Invention]

[0001]

[Field of the Industrial Application] The present invention relates to a display device, and more particularly to a liquid crystal display device capable of lowering a drain leakage current value of a polycrystalline silicon thin film transistor (TFT) and enhancing production efficiency.

[0002]

[Prior Art] In recent years, since a liquid crystal display device has a large advantage of being thin and light-weight and consuming less power consumption, it is progressively used for a display device of OA equipment such as a liquid crystal television, a Japanese word processor and a desktop personal computer. At the same time, development of the liquid crystal display device applying a TFT or a TFT array which uses polycrystalline silicon in an active layer is actively made for the purpose of improving display characteristics.

[0003] Up to now, the TFT which uses polycrystalline silicon in the active layer integrates a switching element and a TFT of a pixel portion as a display portion of the liquid crystal display device and is applied to a driving circuit of the switching element of the pixel portion. That is, it is applied to a TFT of a pixel portion for applying voltage to liquid crystal in a pixel and a TFT of a driving circuit portion for driving the TFT of the pixel portion.

[0004] Development of the present liquid crystal display device is in the direction in which the number of pixels is increased by making the pixel minute and the pixels are operated at high speed. In correspondence with the direction of development, the above-mentioned TFT is required to have the following characteristics.

1) lowering resistance of a gate wiring for eliminating a gate delay.

2) reducing a drain leakage current of the TFT.

[0005] As to 1), a technique is known in which a metal line or silicide is used, for example. In this technique, generally, in order to match a work function with the active layer, a two layer structure is studied in which polycrystalline silicon added with electrical impurity is used as the lower layer and the above-mentioned metal line or silicide is formed as the upper layer to thereby provide low resistance. With this structure, a signal delay due to the gate wiring is reduced.

[0006] As to 2), lowering of the drain leakage current is required for the TFT of the pixel in particular. This is because the drain leakage current is caused on the OFF side of the transistor operation and thus the normal switching function of ON/OFF is not sufficiently provided, and when the above TFT is used in the liquid crystal display device, an electric signal of the pixel cannot be held and thus the contrast is degraded to particularly affect the image quality of the liquid crystal display device. The cause of this drain leakage current is that since electric fields concentrate between the gate and the drain of the TFT, when there is a defect due to a dangling bond in particular, among defects of a silicon bond in the active layer polycrystalline silicon, an abnormal leakage current is caused in a drain joint portion. The reason that the abnormal leakage current is caused in the drain joint portion is as follows. Generally, the source or drain implants ion

necessary for the joint layer with the gate as a mask by an ion implantation apparatus and forms the structure in a self-aligning manner. Therefore, a charge distribution abruptly rises from the gate end. Since a distribution of the electric field is proportional to the charge distribution, the electric field abruptly rises in the vicinity of the drain. Due to this electric field, a tunnel current flows in the channel and the drain joint portion and is observed as the abnormal leakage current.

[0007] As a method of preventing an occurrence of the abnormal leakage current, a technique called LDD (light doped drain) is known. This LDD technique is one in which drain joint is structured by gradually changing the charge distribution in the vicinity of the drain portion. Since the charge distribution gradually changes, a joint electric field in the joint portion gradually changes and the abnormal leakage current does not flow. Therefore, liquid crystal display devices using the polycrystalline silicon TFT manufactured by employing the LDD technique are widely used for a liquid crystal television, OA equipment and the like.

[0008]

[Problems to be solved by the Invention] However, since this LDD technique gradually changes the charge distribution of the joint portion, there is a problem in that generally, a process of implanting ion must be divided into two processes, that is, implantation of the LDD portion at the low concentration and

implantation of the source or drain portion at the high concentration.

[0009] Further, while implantation on the low concentration side is generally performed with a gate mask, implantation on the high concentration side needs to be performed by shifting from a region just under the gate. Accordingly, some mask is necessarily required. Generally, resist, an oxide film, or the like is used for this mask but the manufacturing process becomes inevitably complicated, resulting in a problem in that the manufacturing yield is degraded.

[0010] The present invention has been made in view of solving the above problems. Therefore, an object of the present invention is to provide a liquid crystal display device capable of forming an LDD structure without executing two times of ion implantation and capable of lowering a drain leakage current.

[0011]

[Means for solving the Problem] According to the present invention, a liquid crystal display device comprising at least a thin film transistor (TFT) array substrate having: an insulating substrate; a pixel portion which includes polycrystalline silicon TFTs for switching formed on the substrate; and a driving circuit portion which is formed adjacently to the pixel portion and includes polycrystalline silicon TFTs for driving the pixel portion, is characterized in that the polycrystalline silicon TFTs each have

a gate electrode consisting of a two layer structure of an upper layer and a lower layer, an area of the gate electrode of the lower layer is wider than an area of the gate electrode of the upper layer, and a charge concentration of a polycrystalline silicon layer in a region just under the gate electrode consisting of only the lower layer of the lower layer portion wider than the area of the gate electrode of the upper layer is an intermediate concentration of a channel region and a source or drain region.

[0012] The gate electrode of the polycrystalline silicon TFT according to the present invention consists of the two layer structure of the upper layer and the lower layer. Preferably, the upper layer is composed of a material whose electric resistance value is lower than that of the lower layer. This is because in the case of the two layer structure, the electric resistance value is determined by a layer whose electric resistance is low, and thus it is possible to obtain the low resistance gate electrode by providing a layer comprised of a low resistance material such as a metal compound of silicon as the upper layer. Moreover, the upper layer also functions to hold chemical resistance or heat resistance.

[0013] Further, the lower layer may have the thickness such that in the case of ion implantation for forming the source or drain, the charge concentration of the polycrystalline silicon layer has a concentration gradient and is the intermediate concentration of the channel region and the source or drain region. The other factor

for obtaining the concentration gradient of the charge concentration of the polycrystalline silicon layer is a difference between the dimension of the upper layer shape and the dimension of the lower layer shape. In the present invention, it is preferable that the lower layer has a projecting portion in which the lower layer is projected by several μm from the dimension of the upper layer shape. It is possible to make the charge distribution in the vicinity of the drain gentle by ion implantation with using the above-mentioned gate electrode structure as a mask.

[0014] The liquid crystal display device of the present invention is manufactured as follows. No alkali glass, quartz, or the like can be used for an insulating substrate material. On this substrate, the polycrystalline silicon film is formed by a known method. Namely, an amorphous silicon layer is deposited first on the substrate using a reduced pressure CVD or plasma CVD apparatus, and subjected to heat treatment at a temperature of about 600°C to provide the polycrystalline silicon layer. Thereafter, through a photolithography process and an etching process, the polycrystalline silicon layer is processed into a desired shape. After the surface of the polycrystalline silicon layer is thermally oxidized to form a gate oxide film, a gate wiring consisting of a double film structure is formed thereon. It is preferable that the double film structure is formed by using an etching method in which the etching speed of the upper layer film is faster than that

of the lower layer film. For example, it is preferable to employ RIE (reactive ion etching) using SF_6, CI_2, or the like as a processing gas. Thereafter, the source or drain region is formed in a self-aligning manner with using this gate electrode as a mask. A first interlayer insulating film is formed on the surface and a part of the film is opened as a contact hole. Then, the metal wiring contacts each terminal of the TFT in the hole.

[0015] In order to complete the liquid crystal display device, a second interlayer insulating film is further formed and a contact hole is formed. A transparent electrode is formed therethrogh as a pixel electrode. This substrate is called a TFT array substrate. Thereafter, this TFT array substrate is matched with an opposing substrate and a liquid crystal is injected into the gap portion to thereby compose a liquid crystal cell. Then, an outer assembly is formed to obtain the liquid crystal display device of the present invention.

[0016]

[Operation] The gate wiring of the polycrystalline silicon TFT according to the liquid crystal display device of the present invention is a two layer structure having a low resistance wiring on the upper portion. Since the end portion of the gate wiring is step-like, it is possible to make the charge distribution in the vicinity of the drain gentle by ion implantation in a self-aligning manner with using this gate wiring as a mask. When the charge

distribution in the vicinity of the drain is made gentle, it is possible to prevent the electric fields from concentrating. As a result, the drain leakage current is reduced.

[0017] Moreover, the metal wiring of the upper portion of the gate wiring enables a low resistance gate wiring.

[0018]

[Embodiment] An embodiment of the present invention is described with reference to Figs. 1 to 4. Fig. 1 is a sectional view of a gate portion of a TFT used in a liquid crystal display device of this embodiment. Polycrystalline silicon is formed on a quartz substrate 1 to have a thickness of 1000 angstrom as an active layer 2 of the TFT. As to this polycrystalline silicon active layer 2, disilane gas is used as a material gas, amorphous silicon is formed by reduced pressure CVD, and heat treatment is subjected thereto, to thereby form the polycrystalline silicon. Thereafter, through a photolithography process and an etching process, the polycrystalline silicon is processed into a predetermined shape.

[0019] Next, the surface of the polycrystalline silicon layer 2 is thermally oxidized to form a gate oxide film 3 having a thickness of 700 angstrom. On the gate oxide film 3, a gate wiring having a double film structure is formed by the following method. First, on a lower layer film 4 in contact with the gate oxide film 3, polycrystalline silicon containing $1 \times 10^{19}/cm^3$ of phosphorus (P) as electrical impurity is formed to have a thickness of 1500 angstrom.

Then, as an upper layer film 5, tungsten silicide (WSi) is formed thereon to have a thickness of 2500 angstrom. Next, by an RIE (reactive ion etching) apparatus using SF_6 or CI_2 as an etching gas, it is possible to obtain the gate wiring formed such that the lower layer film 4 is largely projected by 1 to 2 μm from the upper layer film 5, by using a difference of etching rate between the upper layer and the lower layer. A sheet resistance of the lower layer of this gate wiring is about 30 Ω/□ and the sheet resistance of the upper layer is about 5 Ω/□ because the upper layer is comprised of a metal compound of silicon. Accordingly, since the resistance of the double structure wiring is determined by the low resistance, the gate wiring of this embodiment becomes a low resistance gate electrode.

[0020] With using this gate wiring as a mask, ion implantation for forming a source or drain is performed. Phosphorous (P) is implanted by an ion implantation apparatus such that a charge concentration of a portion of 7a shown in Fig. 1 is (5 to 100) x $10^{19}/cm^3$ as an amount of implantation initially determined. Then, acceleration energy of the ion implantation apparatus is adjusted such that the charge concentration of a portion of 7b just under a projecting portion 6 is about 1 x $10^{17}/cm^3$. As a result, as shown in Fig. 1, in the portion 7a where there is no gate, ion implantation of the conventional concentration is executed and the source or drain is formed. In a portion 7c where the gate has a double

structure, ion is not implanted, and in the portion of 7b just under the projecting portion 6, ion at the intermediate concentration is implanted. Thus, the TFT having an electrical impurity distribution can be obtained.

[0021] In the TFT of this embodiment, since a portion where the gate electrode has a double structure is completely masked, the electrical impurity is not implanted. For this reason, the charge distribution in the vicinity of the source or drain of the TFT passes through an intermediate state once without rising abruptly from almost 0.

[0022] Thereafter, as shown in Fig. 2, a first interlayer insulating film 8 is formed and a part of the film is opened as a contact hole. Then, a metal wiring 9 (aluminum (Al)) is made to contact each terminal of the TFT in the hole. Further, a second interlayer insulating film 10 is formed and a contact hole is formed. A transparent electrode 11 is formed therethrough as an electrode of a pixel. This substrate is called a TFT array substrate 12. This substrate 12 is matched with an opposing substrate 13, and a liquid crystal 14 is injected into the gap portion to thereby compose a liquid crystal cell. Then, an outer assembly 15 is formed to complete the liquid crystal display device shown in Fig. 3.

[0023] Characteristics of an n-type TFT of the liquid crystal display device thus obtained are shown in Fig. 4. Fig. 4(a) shows characteristics of the n-type TFT in accordance with this embodiment

and Fig. 4(b) shows characteristics of a conventional example which does not have an LDD structure. A characteristic of a region whose gate voltage is negative is particularly characteristic among them. In the conventional example of Fig. 4(b), in the region whose gate voltage is negative, a drain current greatly leaps up to serve as an extremely large value. On the other hand, in this embodiment of Fig. 4(a), even if the gate voltage changes, the drain current has almost the value 0V of the gate voltage and does not change.

[0024] A first effect of this embodiment is that the number of manufacturing processes can be reduced in comparison with a conventional manufacturing process. That is, by etching adapting the difference in an etching rate once, a step-like projecting portion can be formed in the end portion of the gate electrode. Then, by performing ion implantation using this gate electrode as a mask once, the LDD structure can be provided. Conventionally, ion implantation was performed twice in order to obtain the LDD structure.

[0025] A second effect of this embodiment is that excellent characteristics of the TFT necessary for the liquid crystal display device can be obtained even in the LDD structure manufactured by ion implantation of one time. That is, a drain leakage current has almost the value 0V of the gate voltage but can be made small.

[0026] A third effect of this embodiment is a gate delay is prevented by taking the double structure of the gate wiring and the low

resistance wire.

[0027] According to the above effects, since a leakage current of the TFT is small even if a large number of pixels of 1 million class are operated at high speed on a large-sized substrate, an image quality of the liquid crystal display device is not affected.

[0028]

[Effects of the Invention] In the liquid crystal display device at least comprising the TFT array substrate of the present invention, the polycrystalline TFT has the gate electrode consisting of the two layer structure, and the charge concentration of the polycrystalline silicon layer in the region just under the gate electrode is the intermediate concentration of the channel region and the source or drain region. Therefore, it is possible to obtain the liquid crystal display device comprising the TFT array substrate having a low resistance gate electrode, in which the drain leakage current is low, through a simple manufacturing process. Accordingly, it is possible to enhance production efficiency of the liquid crystal display device. Further, since the number of pixels is increased and the pixels can be operated at high speed, the liquid crystal display device of high image quality can be obtained.

[Brief Description of the Drawings]

[Fig. 1] A sectional view of a gate portion of a TFT used in a liquid crystal display device of this embodiment.

[Fig. 2] A sectional view of the TFT used in the liquid crystal display device of this embodiment.

[Fig. 3] A view showing the liquid crystal display device of this embodiment.

[Fig. 4] A view showing characteristics of the TFT used in the liquid crystal display device of this embodiment.

[Description of Reference Numerals]

1 quartz substrate, 2 active layer, 3 gate oxide film, 4 lower layer film, 5 upper layer film, 6 projecting portion 7a portion with no gate, 7b portion just under projecting portion, 7c portion where a gate has a double structure, 8 first interlayer insulating film, 9 metal wiring, 10 second interlayer insulating film, 11 transparent electrode, 12 TFT array substrate, 13 opposing substrate, 14 liquid crystal, 15 outer assembly